I CLAIM:

1. A memory cell comprising:

a first electrode deposited on a substrate body;

a second electrode, where the first electrode and the second electrode provide access to the memory cell;

a first layer of a silver chalcogenide disposed between the first electrode and the second electrode, where the first layer forms a first portion of a memory cell body; and

a second layer of a chalcogenide glass that forms a second portion of the memory cell body, where the second layer is also disposed between the first electrode and the second electrode, where the chalcogenide glass permits a conductive pathway to form between the first electrode and the second electrode in response to an electric potential applied between the first electrode and the second electrode.

2. The memory cell as defined in Claim 1, wherein the first layer of the silver chalcogenide is formed directly on the first electrode.

3. The memory cell as defined in Claim 1, wherein the second layer of the chalcogenide glass is formed directly on the first electrode.

4. The memory cell as defined in Claim 1, wherein the silver chalcogenide comprises silver selenide.

5. The memory cell as defined in Claim 1, wherein the silver chalcogenide comprises silver sulfide.

6. The memory cell as defined in Claim 1, wherein the silver chalcogenide comprises silver telluride.

7. The memory cell as defined in Claim 1, wherein the silver chalcogenide comprises silver oxide.

8. The memory cell as defined in Claim 1, wherein the chalcogenide glass comprises germanium selenide ($Ge_xSe_{(1-x)}$).

9. The memory cell as defined in Claim 1, wherein the chalcogenide glass comprises arsenic selenide (As_xSe_y).

10. The memory cell as defined in Claim 1, wherein the chalcogenide glass comprises germanium sulfide ($Ge_xS_{(1-x)}$).

11. The memory cell as defined in Claim 1, wherein the chalcogenide glass is selected from the group of chalcogenide glasses that comprise selenium, can be doped with silver, and can remain an amorphous material after the doping with silver.

12. The memory cell as defined in Claim 1, further comprising a third layer of a silver (Ag) that forms a third portion of the memory cell body, where the third layer is also disposed between the first electrode and the second electrode, where the first layer, the second layer, and the third layer are arranged such that the second layer of chalcogenide glass is disposed between the first layer of the silver chalcogenide and the third layer of silver (Ag).

13. The memory cell as defined in Claim 1, wherein at least one of the first electrode and the second electrode comprises tungsten (W).

14. A memory cell comprising:

a first electrode;

a second electrode, where the first electrode and the second electrode provide access to the memory cell; and

a memory cell body disposed between the first electrode and the second electrode, where the memory cell body includes co-deposited silver selenide and germanium selenide ($Ge_xSe_{(1-x)}$).

15. The memory cell as defined in Claim 14, wherein x is in the range of about 0.2 to about 0.43.

16. The memory cell as defined in Claim 14, wherein the germanium selenide ($Ge_xSe_{(1-x)}$) is $Ge_{40}Se_{60}$.

17. The memory cell as defined in Claim 14, wherein the germanium selenide ($Ge_xSe_{(1-x)}$) is $Ge_{25}Se_{75}$.

18. The memory cell as defined in Claim 14, wherein the memory cell body is from about 1:1 to about 5:1 silver selenide to germanium selenide ($Ge_xSe_{(1-x)}$).

19. The memory cell as defined in Claim 14, wherein the memory cell body is from about 1.43:1 to about 2:1 silver selenide to germanium selenide ($Ge_xSe_{(1-x)}$).

20. The memory cell as defined in Claim 14, wherein the memory cell body is from about 1.72:1 to about 1.75:1 silver selenide to germanium selenide ($Ge_xSe_{(1-x)}$).

21. A process of fabricating a memory structure in a substrate assembly, the process comprising:

forming a bottom electrode in contact with a conductive region in the substrate assembly;

forming an active layer on the bottom electrode, where the active layer includes a silver chalcogenide and a selenium-including glass, where the active layer is formed substantially in the absence of an ultraviolet (UV) photodoping step and in the absence of a thermal doping step; and

forming a top electrode layer such that a voltage applied across the top electrode layer and the bottom electrode layer generates an electric field in the active layer.

22. The process as defined in Claim 21, wherein the selenium-including glass is germanium selenide ($Ge_xSe_{(1-x)}$), wherein x is selected from a range of about 0.2 to about 0.43.

23. The process as defined in Claim 21, wherein the silver chalcogenide comprises silver selenide.

24. A physical vapor deposition (PVD) process of fabricating an active layer in a memory cell, the process comprising:

forming a bottom electrode in contact with a conductive region in a semiconductor base material;

depositing both a silver chalcogenide and a chalcogenide glass at the same time on the bottom electrode; and

forming a top electrode layer, where a voltage applied to the top electrode layer and the bottom electrode layer generates the electric field in the active layer.

25. The process as defined in Claim 24, wherein the depositing both the silver chalcogenide and the chalcogenide glass further comprises:

evaporating silver selenide as the silver chalcogenide;

evaporating germanium selenide ($Ge_xSe_{(1-x)}$) as the chalcogenide glass;

introducing the vaporized silver selenide and the vaporized germanium selenide ($Ge_xSe_{(1-x)}$) to the interior of a deposition chamber; and

depositing the vaporized silver selenide and the vaporized germanium selenide ($Ge_xSe_{(1-x)}$) at the same time onto the bottom electrode to form the active layer.

26. The process as defined in Claim 24, wherein x is in a range from about 0.2 to about 0.43.

27. The process as defined in Claim 24, wherein the active layer is deposited such that a ratio of silver selenide as the silver chalcogenide to germanium selenide ($Ge_xSe_{(1-x)}$) as the chalcogenide glass in the active layer is in a range of about 1:1 to about 5:1 by volume.

28. A deposition process of fabricating at least a portion of an integrated circuit, the process comprising:

forming a bottom electrode in contact with a conductive region in a semiconductor base material;

forming a layer of a chalcogenide glass;

forming a layer of a silver chalcogenide, where the layer of the chalcogenide glass and the layer of the silver chalcogenide are adjacent to each other and form an active layer that is capable of supporting the formation of a conductive pathway in the presence of an electric field; and

forming a top electrode layer such that the layer of the chalcogenide glass and the layer of the silver chalcogenide are disposed between the top electrode layer and the bottom electrode layer, where an electric potential applied between the top electrode layer and the bottom electrode layer generates the electric field in the active layer.

29. The process as defined in Claim 28, wherein the layer of chalcogenide glass is germanium selenide ($Ge_xSe_{(1-x)}$), and where the process forms the layer of chalcogenide glass to a thickness within a range of about 200 Angstroms (Å) to about 1000 Å.

30. The process as defined in Claim 28, wherein the chalcogenide glass comprises germanium selenide ($Ge_xSe_{(1-x)}$).

31. The process as defined in Claim 28, wherein the chalcogenide glass comprises arsenic selenide (As_2Se_3).

32. The process as defined in Claim 28, wherein the chalcogenide glass comprises germanium sulfide ($Ge_xS_{(1-x)}$).

33. The process as defined in Claim 28, wherein the silver chalcogenide comprises silver selenide.

34. The process as defined in Claim 28, wherein the silver chalcogenide comprises silver sulfide.

35. The process as defined in Claim 28, wherein the silver chalcogenide comprises silver telluride.

36. The process as defined in Claim 28, wherein the silver chalcogenide comprises silver oxide.

37. The process as defined in Claim 28, wherein the process forms the layer of the chalcogenide glass and the layer of silver chalcogenide by evaporative deposition.

38. The process as defined in Claim 28, wherein the process forms the layer of the chalcogenide glass and the layer of silver chalcogenide by sputtering deposition.

39. A process of forming an active layer in a substrate assembly, where the active layer is capable of supporting the formation of conductive pathways in the presence of an electric potential applied to electrodes, the process comprising:

providing a first amount of germanium selenide ($Ge_xSe_{(1-x)}$) and a second amount of silver (Ag);

depositing the first amount of germanium selenide ($Ge_xSe_{(1-x)}$) and the second amount of silver (Ag);

providing a third amount of silver selenide; and

depositing the third amount of silver selenide.

40. The process as defined in Claim 39, wherein the first amount of germanium selenide ($Ge_xSe_{(1-x)}$) and the second amount of silver (Ag) deposited form a layer that is in a range of about 250 Angstroms (Å) to about 1000 Å thick.

41. The process as defined in Claim 39, wherein the third amount of silver selenide is in a range of about 300 Angstroms (Å) to 1000 Å thick.

42. The process as defined in Claim 39, wherein the first amount of the germanium selenide ($Ge_xSe_{(1-x)}$) and the second amount of silver (Ag) are deposited separately, and where the first amount of germanium selenide ($Ge_xSe_{(1-x)}$) is deposited such that the deposited germanium selenide ($Ge_xSe_{(1-x)}$) lies between the deposited silver (Ag) and the deposited silver selenide.

43. A process of forming an active layer in a substrate assembly, where the active layer is capable of supporting the formation of conductive pathways in the presence of an electric field, the process comprising:

providing silver selenide and no other source of silver (Ag);

providing germanium selenide ($Ge_xSe_{(1-x)}$); and

forming the active layer by combining the silver selenide and the germanium selenide ($Ge_xSe_{(1-x)}$).

44. The process as defined in Claim 43, wherein x is in the range of about 0.2 to about 0.43.

45. The process as defined in Claim 43, wherein the process forms the active layer by combining the silver selenide and the germanium selenide ($Ge_xSe_{(1-x)}$) to a ratio within a range of about 1:1 to about 5:1 silver selenide to germanium selenide ($Ge_xSe_{(1-x)}$) by volume.